



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,076	04/13/2004	Joung-yeal Kim	5649-1229	3985
20792	7590	11/13/2007		
MYERS BIGEL SIBLEY & SAJOVEC			EXAMINER	
PO BOX 37428			MERANT, GUERRIER	
RALEIGH, NC 27627				
			ART UNIT	PAPER NUMBER
			2117	
			MAIL DATE	DELIVERY MODE
			11/13/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

172

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/823,076	KIM ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 August 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 10-13, 21 and 37-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 10-13, 21 and 37-41 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>20071107</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/30/07 has been entered.

### ***Response to Amendment***

2. Applicants' arguments/amendment filed 08/30/07 with respect to claims 1-3, 10-13, 21, & 37-41, have been fully considered but they are not persuasive. The arguments presented are not sufficient to overcome the 35 U.S.C. 112 first paragraph rejections of the claims. Therefore, in view of the 35 U.S.C. 112 first rejections, the Examiner maintains prior rejections of the claims.

3. Claims 4-9, 14-20, and 22-36 have been cancelled.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Art Unit: 2117

5. Claims 1, 10, 11, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitations of comparing the x-bit data output from the nm memory cell arrays to generate nm-bit comparison result data, and outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step are not supported by the specification.

6. Claims 2-3, 12,13, and 37-41 inherit the 35 U.S.C. 112, first paragraph issues of the independent claims 1, 10, 11, and 21 by virtue of their dependency.

In view of the 112 rejections, the Examiner maintains prior rejections:

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1-3, 10-13, 21, and 37-41 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (herein after AAPA).

Claims 1-3: AAPA discloses a method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising: extending y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step (*e.g. [0011, lines last two sentences]*); and comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step (*e.g. [0006] & ([0011], lines 18-26)*).

Claims 10, 39-41: AAPA discloses a method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising: extending y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays wherein nm is integer time as greater as y in a test data write step (*e.g. [0011, lines last two sentences]*); and comparing the x-bit data output from each of the nm memory cell arrays to generate ran-bit comparison result data, grouping and outputting the ran-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal

Art Unit: 2117

lines in response to a control signal, and outputting y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads in a test data read step (e.g. [0006] & ([0011], lines 18-26).

Claims 11-13: **AAPA** discloses a semiconductor memory device comprising nm memory cell arrays configured to respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1 (e.g. items 1-8, fig. 1); a test data write circuit (e.g. item 18, fig. 1) configured to extend y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step (e.g. [0011, lines last two sentences]); and test data read circuit (e.g. fig. 2) configured to compare the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and output y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively (e.g. [0006] & ([0011], lines 18-26).

Claims 21, 37-38: **AAPA** discloses a semiconductor memory device comprising nm memory cell arrays configured to respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1 (e.g. items 1-8, fig. 1);

a test data write circuit (e.g. item 18, fig. 1) configured to extend y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm

Art Unit: 2117

memory cell arrays wherein nm is integer times as greater as y (e.g. [0011, lines last two sentences]);

and test data read circuit (e.g. fig. 2) configured to compare the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and output y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads (e.g. [0006] & ([0011], lines 18-26).

### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10:30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

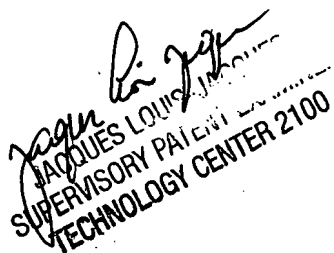
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you

Art Unit: 2117

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Guerrier Merant  
11/07/07



JACQUES LOUIS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100





**UNITED STATES PATENT AND TRADEMARK OFFICE**

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/823,076		2117	21M1

**Correspondence Address / Fee Address Change**

The following fields have been set to Customer Number 20792 on 10/11/2007

- Correspondence Address

The address of record for Customer Number 20792 is:

MYERS BIGEL SIBLEY & SAJOVEC  
PO BOX 37428  
RALEIGH, NC 27627